



STIC Search Report

EIC 3700

STIC Database Tracking Number: 143370

TO: Linda Sholl
Location: RND 8a31
Art Unit: 3700
Monday, March 21, 2005

Case Serial Number: 10/821281

From: Terry Solomon
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RND 8b31
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Search Notes

No past or current litigation found pertaining to US pat. 6439833.

Sources:

Lexis/Nexis
Questel-Orbit

652542 (09) 6439833 August 27, 2002

Time of Request: March 21, 2005 02:19 PM EST

Research Information:

Utility, Design and Plant Patents
patno=6439833

UNITED STATES PATENT AND TRADEMARK OFFICE GRANTED PATENT

6439833

August 27, 2002

V-blade impeller design for a regenerative turbine

REISSUE: April 8, 2004 - Reissue Application filed Ex. Gp.: 3745; Re. S.N. 10/821,281 (O.G. August 3, 2004)

APPL-NO: 652542 (09)

FILED-DATE: August 31, 2000

GRANTED-DATE: August 27, 2002

ASSIGNEE-AT-ISSUE: Delphi Technologies, Inc., Troy, Michigan, 02

ASSIGNEE-AFTER-ISSUE: May 10, 2001 - ASSIGNMENT OF ASSIGNEES INTEREST (SEE DOCUMENT FOR DETAILS)., DELPHI TECHNOLOGIES, INC. P.O. BOX 5052 LEGAL STAFF- MAIL CODE : 480-414-420 TROY MICHIGAN 48007, Reel and Frame Number: 11792/0413

LEGAL-REP: Cichosz, Vincent A. - ##0

Selected file: PLUSPAT
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** SS 1: Results 1
PRT SS 1 MAX 1 LEGALALL

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Patent Number :

US6493833 B1 20021210 [US6493833]

Title :

(B1) Microcomputer

Patent Assignee :

(B1) MITSUBISHI ELECTRIC CORP (JP)

Patent Assignee :

Mitsubishi Denki Kabushiki Kaisha, Chiyoda-Ku [JP]

Inventor(s) :

(B1) UTSUMI TAKASHI (JP)

Application Nbr :

US44005699 19991115 [1999US-0440056]

Priority Details :

JP13268599 19990513 [1999JP-0132685]

Intl Patent Class :

(B1) G06F-011/27

EPO ECLA Class :

G06F-011/26S2

US Patent Class :

ORIGINAL (O) : 714030000; CROSS-REFERENCE (X) : 703028000 714036000

Document Type :

Basic

Citations :

US5463766; US6075941; US6079016; US6154837; JP1-201762

Publication Stage :

(B1) U.S. Patent (no pre-grant pub.) after Jan. 2, 2001

Abstract :

A microcomputer including a built-in storage portion capable of executing an evaluation program by an ICE through a simple operation also when the evaluation program cannot be written in the built-in ROM is obtained. A debugging circuit (2) outputs a reset vector selection signal (S2) indicating generation of a reset vector (V1/V2) in response to a control signal (S1) indicating a normal mode/a RAM starting mode, and a reset circuit (3) generates a reset vector (V1/V2) indicating a starting address (A1/A2) after reset cancellation by indication of the reset vector selection signal (S2). The microcomputer can be set to execute the evaluation program from the starting address (A2) on a RAM area (5) after reset cancellation by registering the evaluation program (start address=starting address (A2)) in the RAM area (5) from the ICE through the debugging circuit (2) and thereafter supplying a control signal (S1) indicating the RAM starting mode to the debugging circuit (2).

Update Code :

2002-51

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Patent Number :

US6493833 B1 20021210 [US6493833]

Application Number :

US44005699 19991115 [1999US-0440056]

Action Taken :

19991115 US/AS-A

ASSIGNMENT

OWNER: MITSUBISHI DENKI KABUSHIKI KAISHA 2-3, MARUNOUCHI; EFFECTIVE
DATE: 19991101
ASSIGNMENT OF ASSIGNORS INTEREST;ASSIGNOR:UTSUMI,
TAKASHI;REEL/FRAME:010402/0521

Update Code :

2004-25

Session finished: 21 MAR 2005 Time 20:48:27
QUESTEL.ORBIT thanks you. Hope to hear from you again soon.